REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance: None of the prior art of record teach or suggest a mold for molding a semiconductor device package, comprising: a cavity block, the cavity block comprising a concave surface defining a cavity in which a semiconductor chip may be positioned, the semiconductor chip being generally rectangular and comprising a top surface, bottom surface, and four side surface; a gate, the gate defining a mold resin entry into the cavity and having a gate width; and a gate block arranged and configured for movement relative to the cavity block to provide selective opening and closing of the gate; wherein the gate is arranged relative to the semiconductor chip whereby mold resin entering the cavity through the gate will contact two closest side surfaces of the semiconductor chip, flow substantially parallel to the top and bottom surfaces, at an angle of less than about 70 degrees. The closest prior art Suetaki discloses a mold wherein the resin flow upward relative to the chip as illustrated in figure 6. The 112 rejection has been withdrawn as discussed in the interview summary as the language regarding parallel to the chip was only added to clarify the angle with which the resin contacts the chip within the mold cavity.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert B. Davis whose telephone number is 571-272-1129. The examiner can normally be reached on Monday-Friday 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yogendra Gupta can be reached on 571-272-1316. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Robert B. Davis/
Primary Examiner, Art Unit 1791
2/19/08